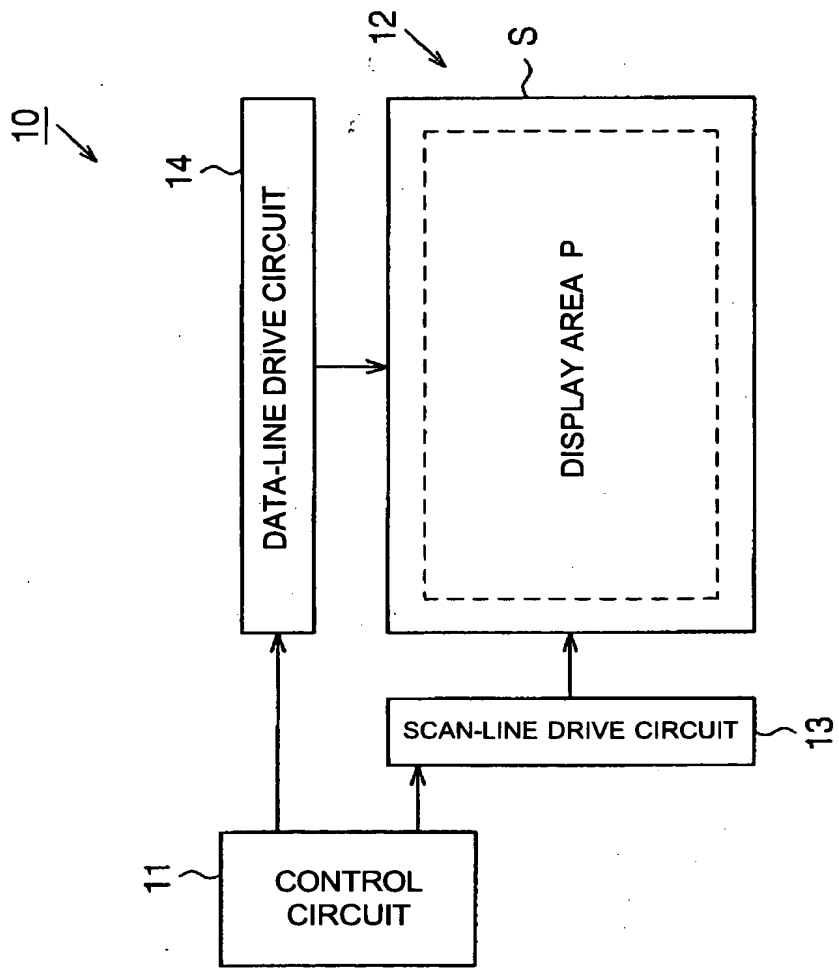
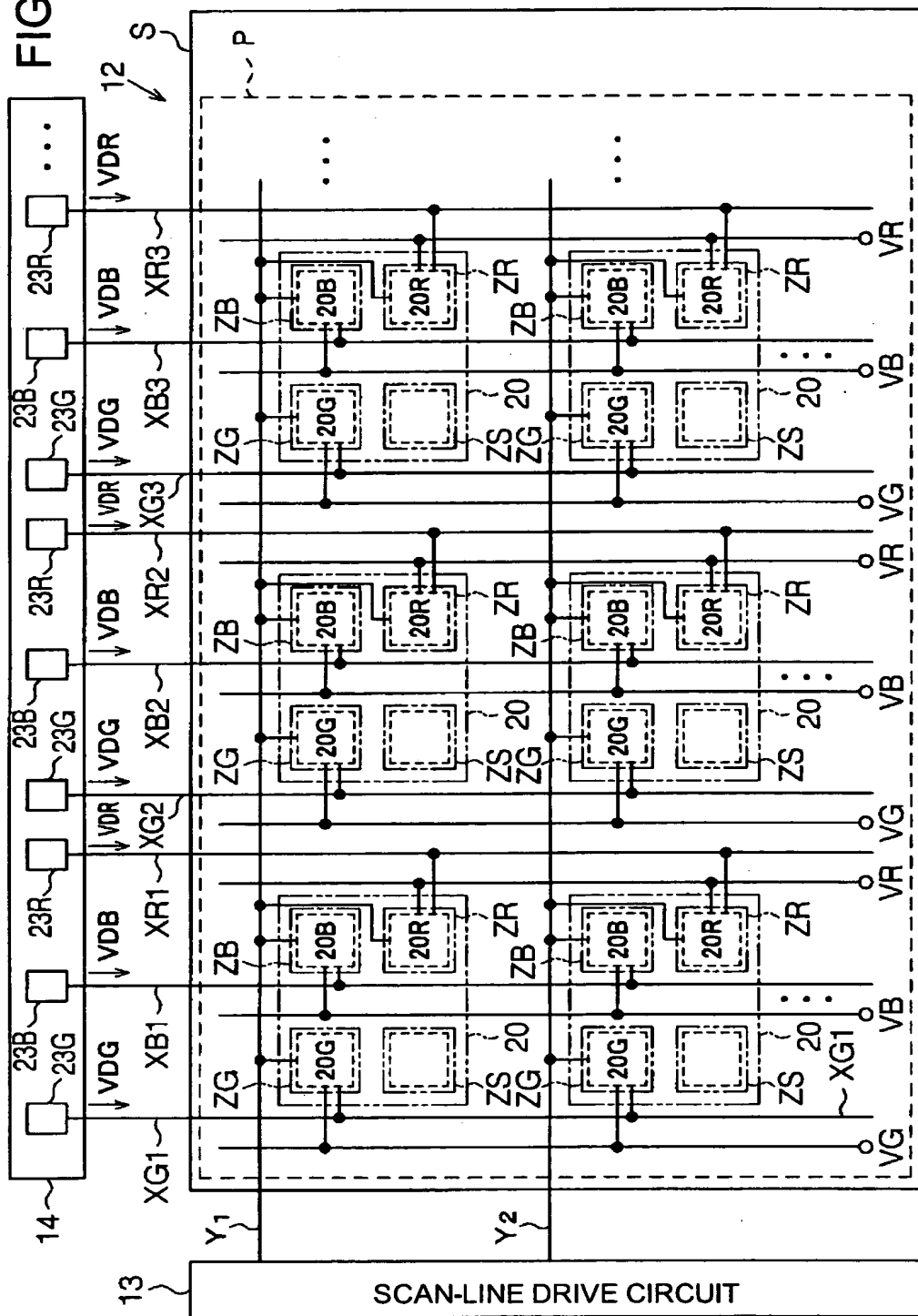


FIG.1



**FIG. 2**



**FIG. 3**

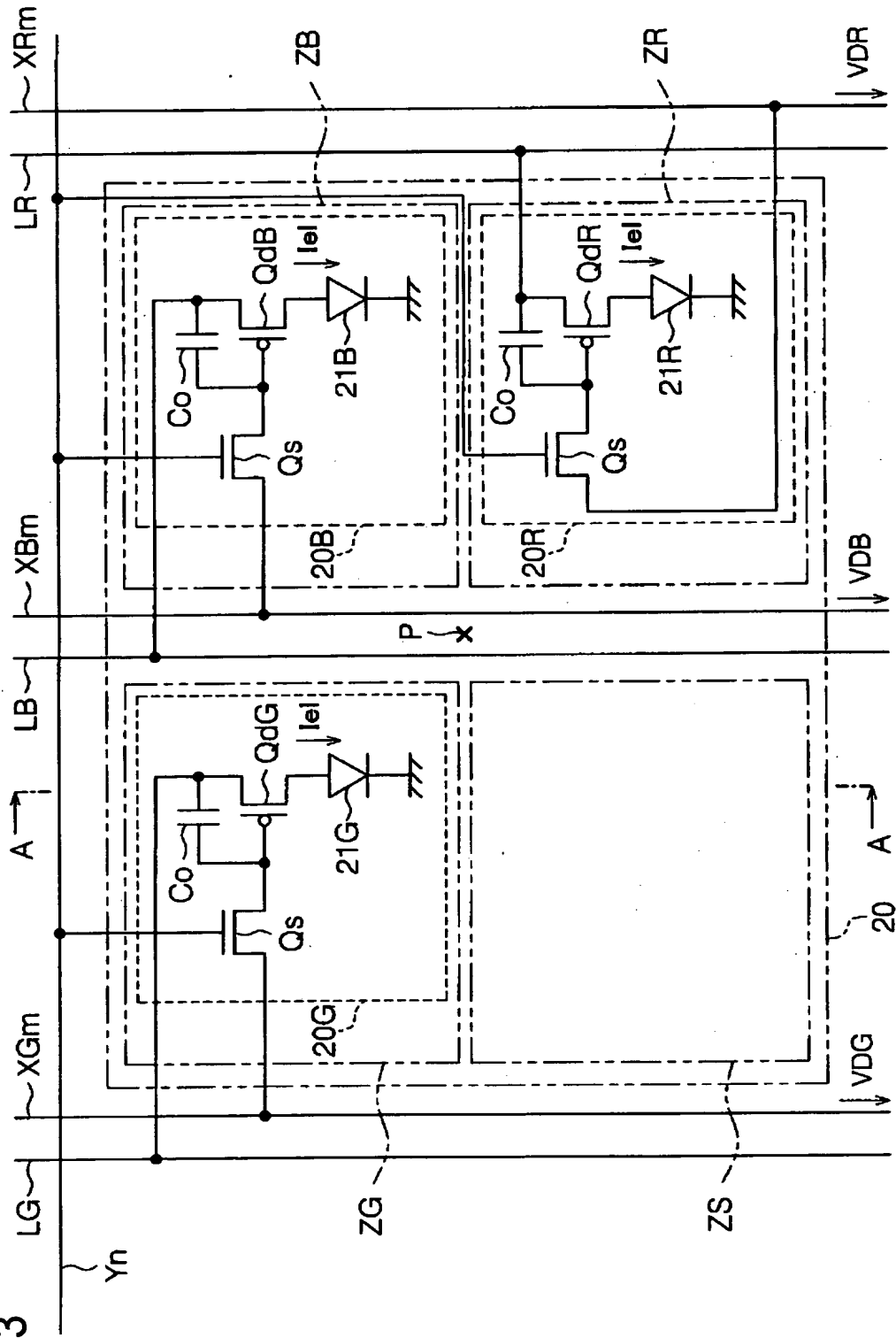


FIG.4

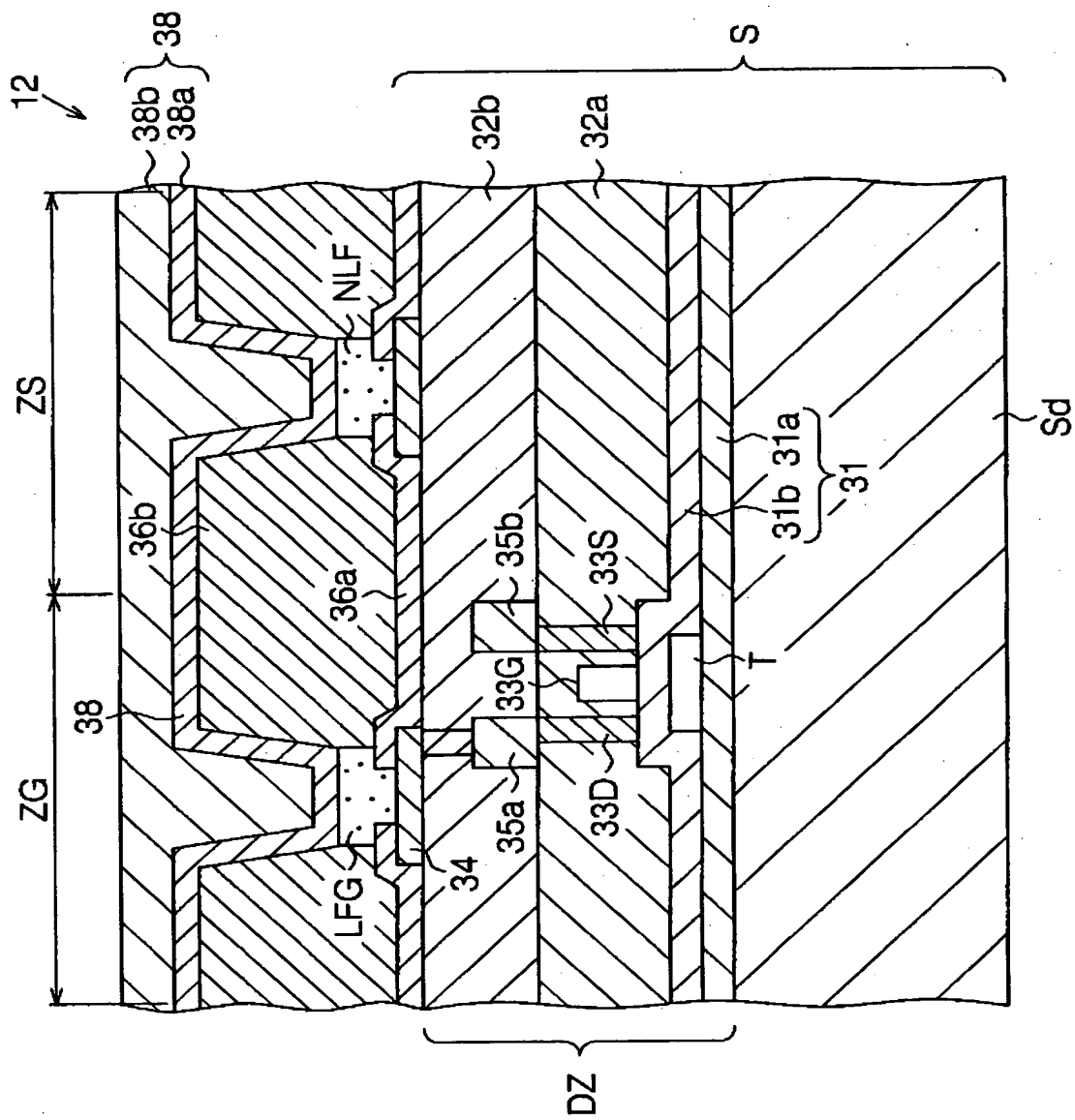
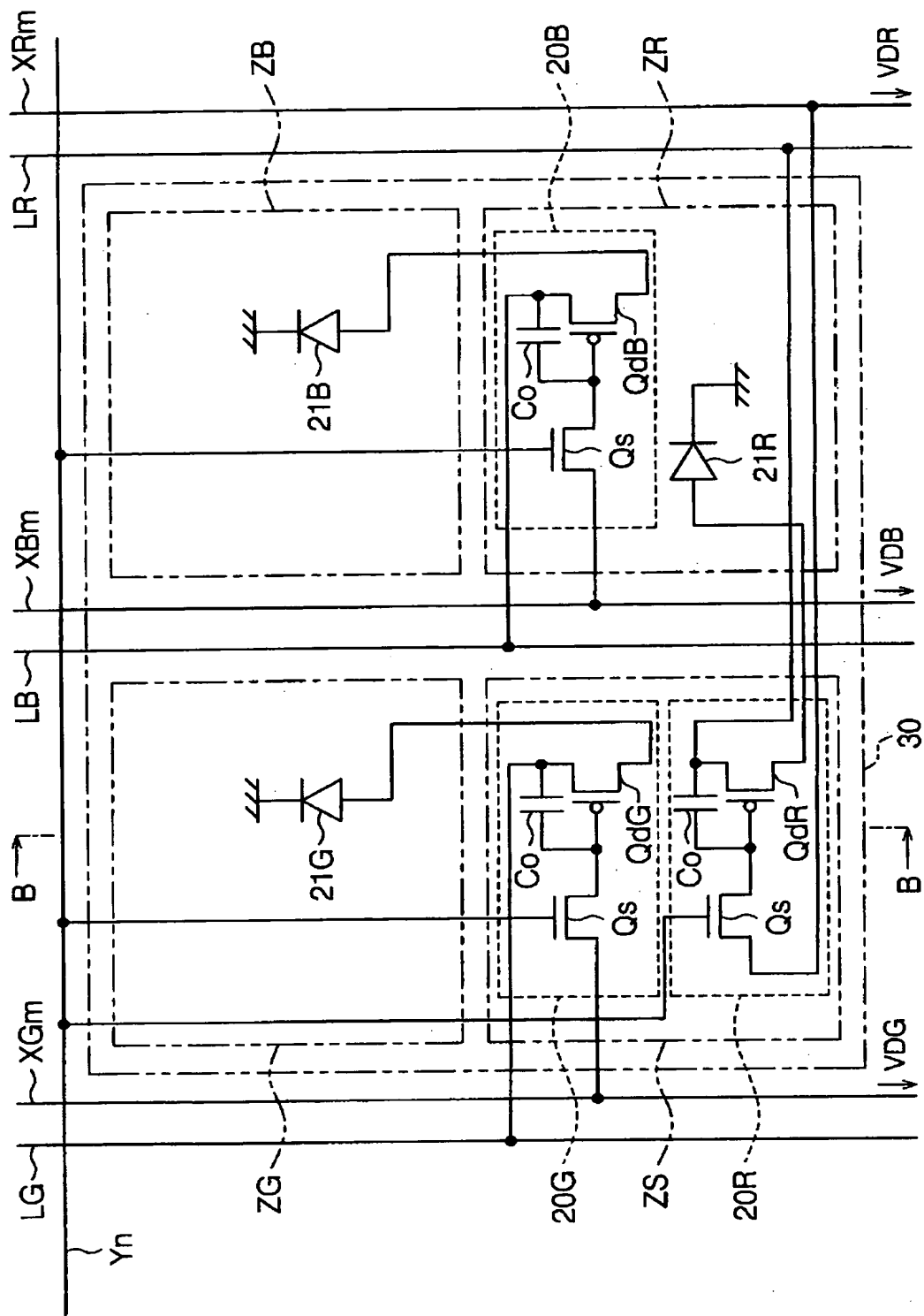


FIG.5



This cross-sectional diagram illustrates a multi-layered semiconductor structure. The substrate is labeled Sd. A series of layers are shown, including a bottom layer 31 (comprising 31a and 31b), followed by a layer T. Above this is a stack of alternating conductive and insulating layers, with labels 33D, 33S, 33G, 35a, 35b, 36a, 36b, 38a, and 38b. A central region is labeled NLF. The top surface is indicated by 12. Dimensions ZG, ZS, and DZ are marked along the vertical axis.

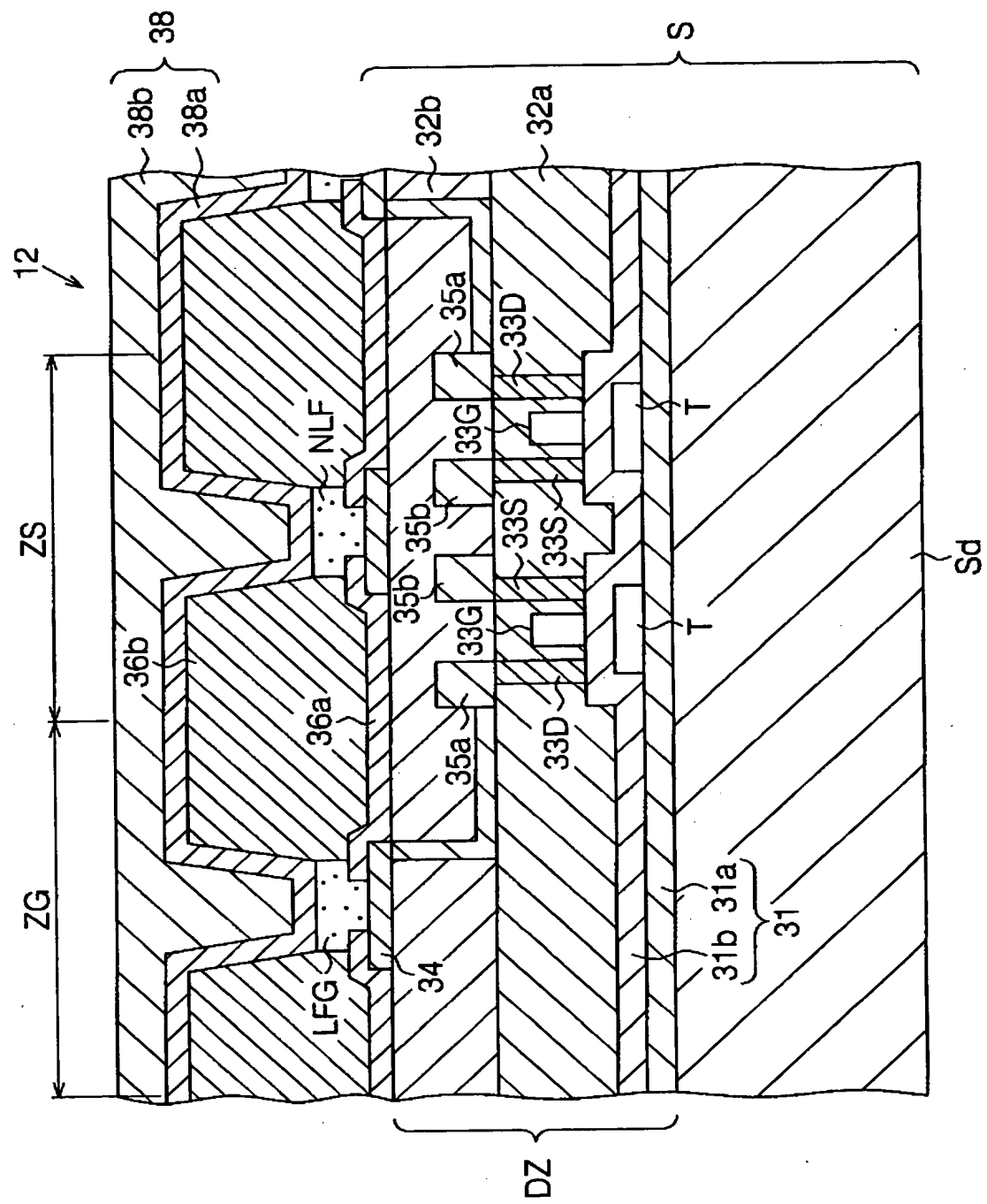


FIG.7

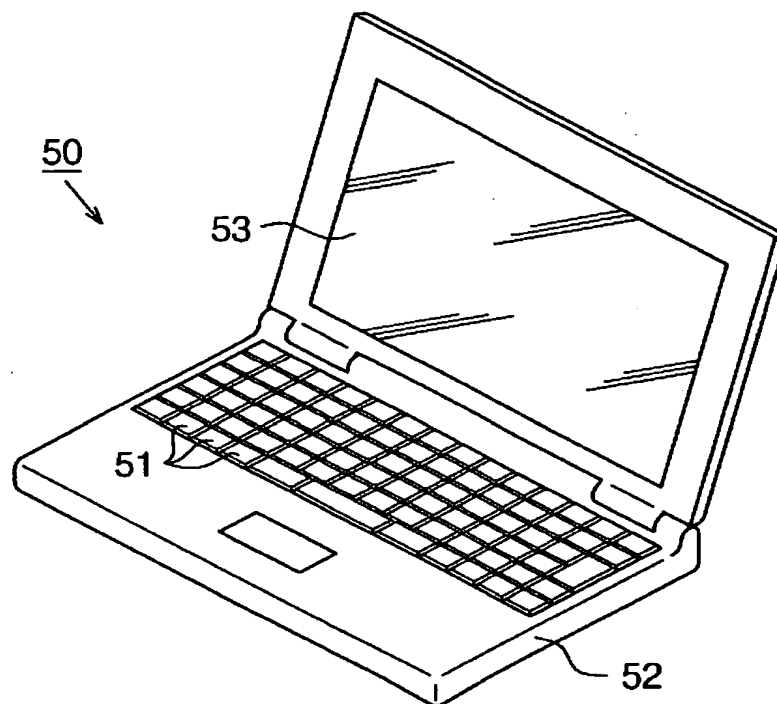


FIG.8

